

WHAT WE CLAIM ARE:

1. A semiconductor device comprising:
 - a semiconductor substrate having a principal surface;
 - a fuse circuit formed above the principal surface, said fuse circuit
 - 5 having fuse elements each having a predetermined breaking point;
 - a first trench isolation region formed in a surface layer of said semiconductor substrate under said fuse circuit; and
 - a plurality of active region dummies formed through said first trench isolation region in an area excepting a predetermined area around the
 - 10 predetermined breaking point.
2. A semiconductor device according to claim 1, further comprising a silicide layer covering at least one of said active region dummies.
- 15 3. A semiconductor device according to claim 1, further comprising a plurality of insulating films each covering a semiconductor surface of an associated one of said active region dummies.
4. A semiconductor device according to claim 1, further comprising a continuous
- 20 insulating film covering semiconductor surfaces of said active region dummies.
5. A semiconductor device according to claim 1, further comprising:
 - a second trench isolation region formed in the surface layer of said semiconductor substrate in an area different from said fuse circuit;
 - 25 an active region formed through said second trench isolation region;

and

a main circuit including a MOS transistor comprising an insulated gate electrode formed traversing on a surface of said active region, source/drain regions formed in said active region on both sides of said insulated gate electrode,
5 and silicide layers formed on surfaces of said source/drain regions.

6. A semiconductor device according to claim 1, further comprising a gate electrode dummy formed on at least one of said active region dummies.

10 7. A semiconductor device according to claim 1, wherein said predetermined area is a region having a predetermined radius.

8. A semiconductor device according to claim 1, further comprising a plurality of wiring layers having a via conductor and a wiring pattern, wherein said fuse circuit
15 is surrounded by a guard ring made of the same layers as layers of the via conductor and the wiring pattern.

9. A semiconductor device comprising:

a semiconductor substrate having a principal surface;
20 a fuse circuit formed above the principal surface, said fuse circuit having fuse elements each having a predetermined breaking point;
a first trench isolation region formed in a surface layer of said semiconductor substrate under said fuse circuit;
a plurality of active region dummies formed through said first trench
25 isolation region; and

an insulting film covering a semiconductor surface of said active region dummies.

10. A semiconductor device according to claim 9, further comprising:

5 a second trench isolation region formed in the surface layer of said semiconductor substrate in an area different from said fuse circuit;

 an active region formed through said second trench isolation region;
and

 a main circuit including a MOS transistor comprising an insulated
10 gate electrode formed traversing on a surface of said active region, source/drain regions formed in said active region on both sides of said insulated gate electrode, and silicide layers formed on surfaces of said source/drain regions,

 wherein semiconductor surfaces of said active region dummies have no silicide layer.

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